

4/16/04
FORM PTO-1449 (MODIFIED)

LIST OF PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENT

Applicant: Diodato et al.
Case: 9-7-17-2
Serial No.: 09/865,847
Filing Date: May 25, 2001
Group: 2185

U.S. PATENT DOCUMENTS

EXAMINER	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE	IF APPROPRIATE
<u>C</u>	5,737,746	04/07/098	Hardin et al.		711/118	

FOREIGN PATENT DOCUMENTS

EXAMINER	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	TRANSLATION	YES	NO

OTHER DOCUMENTS

EXAMINER	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.

Examiner CPD

Date Considered 7/20/04

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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FORM PTO-1449 (MODIFIED)
LIST OF PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENT



5/31/02
Applicant: Kaxiras et al.
Case: Diodato 9-7-17-2
Serial No.: 09/865,847
Filing Date: May 25, 2001
Group: 2185

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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS

JUN 04 2002

Technology Center 2100

C Burger et al., "The Declining Effectiveness of Dynamic Caching for General-Purpose Microprocessors," University of Wisconsin-Madison, CS TR #1261, (1995).

C Powell et al., "Gated- V_{dd} : A Circuit Technique to Reduce Leakage in Deep-Submicron Cache Memories," Purdue University, ISLPED '00, Rapallo, Italy, (2000).

C Wood et al., "A Model for Estimating Trace-Sample Miss Ratios," Proc. of ACM Sigmetrics Conf. on Measurement and Modeling of Computer Systems, (May 1991).

C Yang et al., "An Integrated Circuit/Architecture Approach to Reducing Leakage in Deep-Submicron High-Performance I-Caches," Proc. of the Seventh Int'l Symposium on High-Performance Computer Architecture (HPCA), (2001).

Examiner

CAV

Date Considered 7/20/04

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